LOWER HYBRID LOW POWER MICROWAVE ACTIVE CONTROL SYSTEM DESIGN, INSTALLATION AND TESTING ON ALCATOR C-MOD

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***Abstract*. Current profile evolution will be controlled and sustained in the Alcator C-Mod Advanced Tokamak Lower Hybrid Current Drive Experiment by use of 3 MW of 4.6 GHz Lower Hybrid Current Drive (LHCD) now being installed and tested. LHCD and an existing 5MW ICRH capability are to be used to develop regimes with high confinement, high β_n and high bootstrap fraction and extend them to quasi-steady-state conditions. This paper will describe the design, installation and testing of the low power microwave active control system used in the experiment. The LHCD low power microwave active control system uses vector modulators to provide a phase and amplitude controlled driver for each of twelve 4.6 GHz, 250kW klystrons. Phase and power output of each klystron are monitored by an I-Q detector and the resulting signals are used in digital controllers for closed-loop control of the klystron phase and amplitude to preset values.**

I. INTRODUCTION

The lower hybrid current drive (LHCD) system being installed on the Alcator C-Mod tokamak will allow research in advanced tokamak (AT) physics operation [1]. Three MW of power at 4.6 GHz will be available for a maximum pulse length of 5 s, with power being provided by twelve 250 kW Varian model VKC-7849 klystron amplifiers. Two adjacent columns of the 4 by 24 waveguide array launcher will be powered by each klystron, and low power driver signals for each klystron amplifier will be actively phase and amplitude controlled to match the phase of the launched power to the plasma $n_{||}$ spectrum for LHCD experiments [2].

Synchronized digital controllers have been designed using off-the-shelf hardware and software. Used in conjunction with the low power microwave circuitry (LPMC) and in-house interfacing, timing and logic circuit designs the controllers will provide 24 channels of deterministic real-time control for the 12 klystron systems. While in-phase and quadrature (I-Q) vector modulators and I-Q detectors form the basis of the klystron drive and monitoring system in the LPMC, fast external protection for the klystrons is provided by the Transmitter Protection System (TPS) [3]. Digital controller operation is closely coordinated with the TPS and the system design allows remote phase and amplitude setpoint waveform entry as well as gain and other parameter entry.

II. CONTROL SYSTEM COMPONENTS

Fig. 1 shows the LPMC, Active Control System (ACS) and one of twelve high power microwave circuits. The control system may be described in terms of its subsystems: the LPMC, the ACS, and auxiliary timing, logic and interface circuitry.

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A. LPMC

The LPMC contains the 4.6 GHz microwave circuits used for generating the klystron amplifier drive signals and monitoring the results.

The LHCD microwave signal originates in a CTI, Inc. solid-state phase-locked source with frequency stability of ± 5 ppm and an output power of +15 dBm. The oscillator output is isolated from reflections, amplified to +27 dBm, and split by a two-way divider to supply the driver and monitoring circuits. Two sixteen-way dividers further divide the signal into twelve drive and monitoring circuit legs.

Each of twelve drive legs controls the microwave power and phase using a G.T. Microwave I-Q vector modulator (VM) over a 20 dB and 360° range with 12-bit resolution. Adjustable phase shifters and attenuators in series with each VM compensate for varying path lengths and losses among the different klystrons, and an output amplifier makes up for the VM's 12 dB insertion loss and drives a low-loss coaxial cable connecting to a PIN switch. This TPS-controlled switch and final 30 dBm output preamplifier are located at the klystron.

I-Q phase detectors (MITEQ Model IQM4.6LC1) generate I and Q voltages and are used to determine the phase between the reference oscillator and a feedback signal. The 16-way divider provides local oscillator (LO) reference signals for each I-Q detector and a variable attenuator is used to adjust the pick-off power to a -2 dBm maximum at the detector input for full klystron output power. A microwave switch circuit allows each high power circuit feedback point to be selected from either the klystron output directional coupler or the launcher input directional coupler. The klystron feedback point allows transmitter system tests without launcher involvement.

B. ACS

The preliminary ACS design, described in a previous paper, has evolved, with both hardware and software improvements being realized [4]. The ACS allows deterministic real-time control with a 1 ms response to changes when operated in a limited closed-loop mode. A Linux workstation is used between LHCD pulses to enter the desired amplitude and delta phase setpoint waveforms, limits and loop gains. Since the VM and I-Q phase detectors use I-Q signals to set and detect klystron phase and amplitude, the design uses 12 synchronous I-Q control-loop pairs, eliminating conversion of I-Q values to phase and amplitude values during real-time operation.

One amplitude and one delta phase waveform is entered for a 5 s LHCD pulse and the data computer calculates twelve amplitude and phase setpoint waveforms. The amplitude waveform entered is used for all twelve amplitude waveforms and the delta phase waveform sets the difference in phase between adjacent launcher column pairs. Twelve I and twelve Q setpoint waveforms are generated for use in the ACS

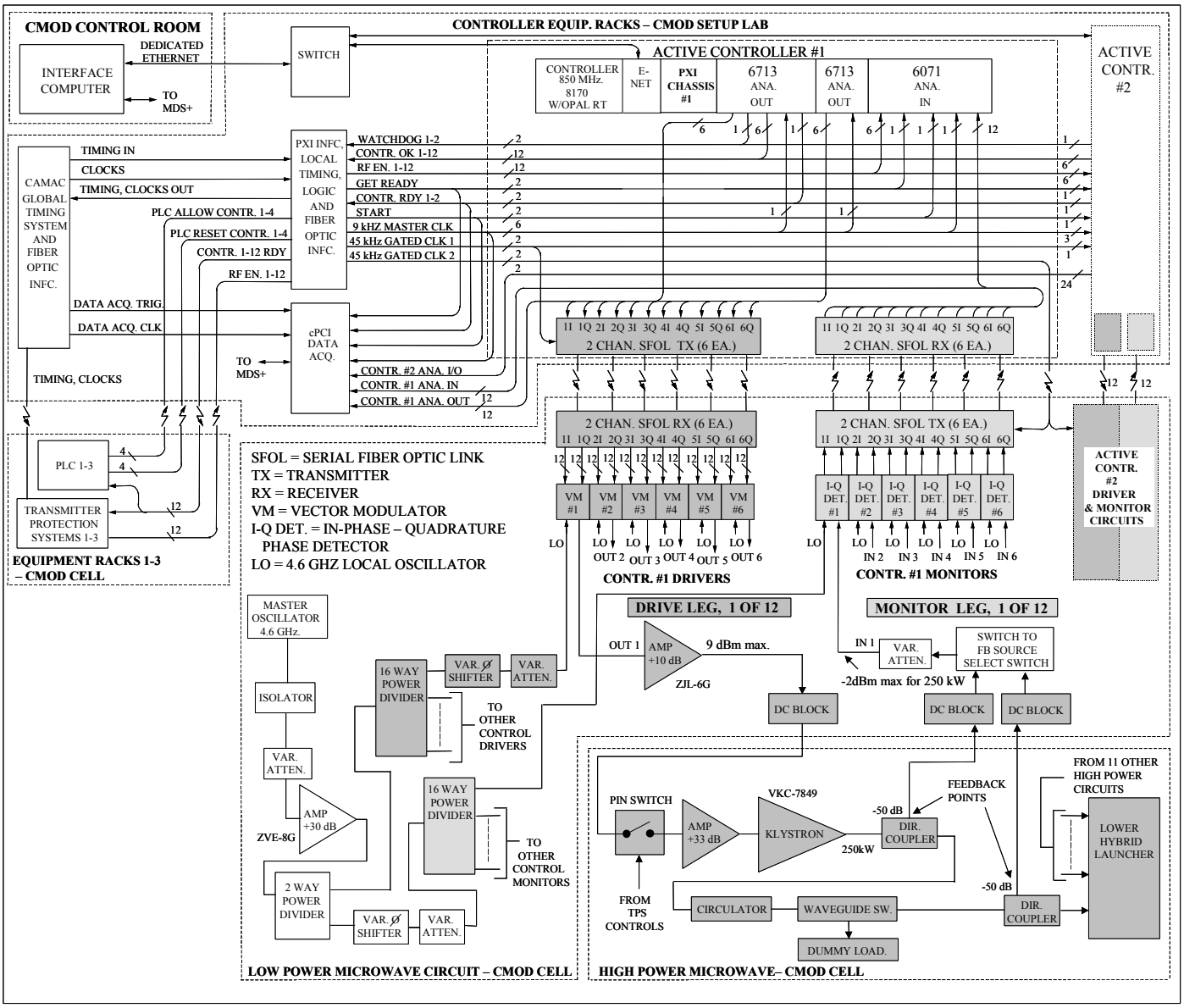

Fig. 1 System Block Diagram

proportional-integral-derivative (PID) loops with each waveform also being separately editable.

Limit windows around setpoint waveforms and feedback inputs restrict the range of controller output commands and allow the ACS to provide slow fault response. Open-loop mode is used in all control loops for the first few ms and after a fault to allow the klystron outputs to reach the setpoint values and provide reasonable feedback input levels before the loops are closed. In open-loop mode, the waveforms are used to calculate control outputs directly.

1) Controller Hardware

A Windows interface computer with dedicated Ethernet is provided for communication to two identical active controllers and also communicates with the MDS+ data system over a separate Ethernet link. An MDS+-compatible cPCI data acquisition system acquires controller I-Q analog input and output (I/O) and timing data [5]. Active controller chassis 1 and 2 will communicate with the LPMC VM and I-Q phase detectors over 24 dual-channel serial fiber-optic link (SFOL) transmitter and receiver modules [6].

To meet the real-time control requirements, we designed a system based on two synchronized National Instruments PXI chassis, each with an 850 MHz model 8170 controller, Ethernet module, 6071E analog input module and two 6713 analog output modules. Analog I/O modules also provide the required digital I/O. The 6071E analog input module analog-to-digital (A/D) converter has 12-bit resolution and supports conversion at 1.25 MS/s. Twelve of its multiplexed differential analog inputs are used to acquire feedback data. The module's hardware timers support acquisition timing and are synchronized by the external local timing system GET READY, MASTER 9 kHz CLOCK and START input signals to the other controller chassis, TPS and PLC controls and C-Mod shot cycle. The MASTER 9 kHz CLOCK is connected to

each of the 6071E and 6713 modules' PFI1/Trig inputs for synchronization and each 6713 analog output module provides six simultaneous 12-bit analog outputs when the MASTER 9 kHz CLOCK pulse is received. Six RF ENABLE signals are input to the controller via the 6071E digital inputs and provide the status of the TPS-controlled PIN switch used to switch the klystron's driver on or off. The WATCHDOG, CONTROLLER READY and six CONTROL OK signals are output by one 6713 module. Each CONTROL OK signal is interlocked to the TPS to turn off the klystron driver if the I-Q control loop pair is not okay. A WATCHDOG output toggles at each program step and allows disabling of the associated klystrons if the system program hangs up.

2) Controller Software

For software development we are using OPAL-RT Technologies' RT-LAB. This software allows development of control models using Mathworks Simulink with Stateflow blocks and provides tools to separate the models and run them on single or parallel personal computers running the QNX Real-Time operating system. Our design requires two master control models that are identical except for naming and addressing. An RT-LAB operator interface provides dialog boxes to allow compilation, distribution and execution of models. The models developed in Simulink and Stateflow are separated into remote and target computer blocks by RT-LAB and then Mathworks Real-Time Workshop, Stateflow Coder code-generation and QNX compilation tools are used to convert the separated models into executables optimized for real-time execution [7].

A LabVIEW program running under Windows mitigates the communication between the C-MOD MDS+ data repository and the two active controllers running QNX and RT-LAB. This LabVIEW program interrogates MDS+ to determine if a shot is about to take place and then reads the I-Q setpoint waveforms and sends them via a LabVIEW to RT-LAB communication layer over a dedicated network. A future goal is to have the active controller programs communicate directly with the MDS+ data servers for both state and settings. This would greatly simplify the system and make it more robust. Two issues with making this change are that the MDS+ network library must be ported to QNX and the RT-LAB software will need to be extended to use this library.

A Stateflow block is used for state control. The block checks for the GET READY hardware input and then loads the waveform setpoint files into memory before the shot. When this is done the CONTROLLER READY hardware output is made true and the program then waits in a tight loop until the START hardware input is received. The first MASTER 9 kHz CLOCK pulse is synchronized to the START pulse and the analog I/O are initiated simultaneously. All 12 analog outputs for each controller are clocked in parallel while a single 12-bit A/D converter running at 1.25 MS/s with 12 multiplexed inputs in each controller converts the analog signals in 9.6 us (1S/1.25 MS/s/Ch.*12Ch.). When the analog inputs are read the model calculates output values based on a velocity PID algorithm and then reads, processes and writes additional digital inputs and outputs. Total time required is less than 111 us, allowing the use of a 9 kHz external clock to run all loops synchronously.

During real-time operation each controller uses digital inputs and outputs to communicate with the TPS. If a klystron driver is switched off by the TPS, the RF ENABLE input causes the controller's I-Q control loop pair to be set to limited open-loop operation to prevent integrator windup. If the TPS enables the klystron again during the pulse, the associated control loop pair is switched back to closed-loop operation after a few ms. CONTROLLER OK outputs notify the TPS that the control loop pairs are not working to allow corrective action. The model leaves real-time mode of operation if the START signal goes false or when the maximum 5 s LHCD pulse time is complete.

3) Operator System Software (OS)

The main component of the OS is a graphical user interface made using Interactive Data Language (IDL) running on a Linux platform. From the lower hybrid control system (LHCOSY) user interface the operator can construct amplitude and phase setpoint waveforms for the klystrons, establish the timing sequence, and acquire and calibrate raw data. All controller parameters such as gains, scaling and limits are stored in the MDS+ data system.

C. Auxiliary Timing, Logic and Interface Circuitry.

The global CAMAC timing system with MPB encoders and decoders uses Jorway 221 timing modules to supply synchronization with C-Mod. A local timing system was designed to provide the MASTER 9 kHz CLOCK, 45 kHz GATED CLOCKS, START and GET READY signals to the controllers and is synchronized by the global timing system. General purpose CPLD modules are used to realize the local timing, fast control logic and microwave safety interface circuit requirements. We standardized on the Atmel ATF1508 CPLD, which has provision for up to 64 I/O lines and 128 macrocells (6000 gates). Programs are developed using the free Windows version of the Universal Compiler for Programmable Logic (WinCUPL), a mature text-based logic description language. The CPLD can be programmed, erased and reprogrammed while on the board. The module designed has flexible I/O circuits, allowing each of the twelve twin LEMO front panel connectors to be used as an optically-coupled input or a 5V buffered output for the CPLD I/O lines. Each module has a 6U, 4HP Euro front panel, but the board design is arranged such that the I/O circuit section is adjacent to the front panel and can be cut off and stacked along with additional front panels onto the CPLD board for a total of 36 front panel connectors. Short ribbon cables connect the stacked I/O board sections to the CPLD board and remaining CPLD I/O may be jumped to pins on the backplane chassis connectors. The board also has a PIC16C505 microcontroller.

A PXI interface system (PXIIS) was designed to allow convenient interconnection of ACS components to the National Instruments PXI controller analog and digital I/O signals and provides optical isolation and signal buffering of digital signals. The PXIIS comprises a 6U, 84HP Euro chassis with four 6U, 8HP interface modules for each of the two active controllers; two each for the 6071E PXI card and one for the two 6713 PXI cards. Each module uses two 64 pin DIN

connectors at the backplane for power and signaling and includes a main board and PXI connector interface board. The main board provides digital signal optical isolation and 5 V output buffering to front panel connectors. The PXI connector interface board provides a PXI cable fanout to allow jumper configuration of analog and digital I/O signals for the PXI card being connected. Fiber-optic interface circuitry allows isolated coordination of controller fault response with that of the TPS and associated programmable logic controller.

III. TESTING

Functional testing of the LPMC rack is complete except for the SFOL modules, and tests have been done on both drive and monitoring circuits. A Matlab program and test circuits are being developed to facilitate automated testing and calibration of microwave circuit channels and allow a National Instruments PXI controller to set the VM I-Q commands using two twelve bit words, read the gain and phase from an Agilent Model 8753ES network analyzer and read the I-Q detector outputs. The program allows the operator to enter a fixed attenuation, start phase, phase increment and end phase for one VM channel and then calculates the I-Q equivalents for the entered phase and amplitude commands. A fixed attenuation scan of from 0 to 360 degrees in one degree increments is being done for numerous fixed attenuation levels and then the I-Q detector and network analyzer data is compared to the commanded phase and amplitude. Since the I-Q detector data is in millivolts, the data must be converted to phase and amplitude to compare to the network analyzer data and commanded phase and amplitude.

A. VM Drive Leg Tests

To test each drive leg, Port 1 of the network analyzer was substituted for the master oscillator at 0dBm output and Port 2 was connected at the LPMC output. With the VM command set to 0 dB attenuation and 0 degrees, the drive leg variable phase shifter and attenuator were used to set the output to 9 dBm at 0 degrees, the desired maximum level before output amplifier saturation. The VM has 12 dB insertion loss and its input was set to 9dBm. Data was taken for 0 to 360 degree phase scans with 1 degree increments for fixed attenuation over the range of 0 to 27 dB in 3 dB steps. Phase error for a typical channel with 0 to 15 dB attenuation commanded was found to be +/- 3.5 degrees with amplitude error being +/- 0.4 dB. For 18 to 27 dB attenuation commanded the phase error was found to be +3 to –14 degrees. Amplitude errors for 18 to 27 dB range from +0.7 to –1.75 dB with largest errors being found at 27 dB attenuation.

B. Monitor Leg Tests

Tests for the monitor leg were done using a loop back from channel drive leg output to channel monitor leg input. The test setup of network analyzer Port 1 was the same as for the drive leg tests. With VM commands at 0 dB attenuation and 0 degrees, the local oscillator (LO) input and RF input to the I-Q detector were both set to 10 dBm at 0 degrees using the network analyzer and variable phase shifter and attenuator. Port 2 was then connected to a –10 dB directional coupler at the input of the I-Q detector and data was taken for scans identical to those in the drive leg. Best results were obtained at I-Q detector inputs less than –2dBm (12 dB VM attenuation) due to detector saturation at higher levels. Over the detector input range of –2 dBm to –17 dBm the phase error was –3 to +6 degrees with amplitude errors of -0.1 to 1.5 dB.

C. Calibration Plans

Work has started on calibration of the drive and monitoring legs. We plan to repeat the monitor leg tests using VM commands that have been compensated according to the drive leg test results. This will provide a more accurate characterization of the I-Q detectors. Data being taken for the 12 channels will be used in the calibration program being developed to compensate for system errors due to VM and I-Q detector non-linearity.

IV. STATUS

ACS system designs are being completed and testing of the active controllers, PXI Interface, local timing and serial fiber optic links (SFOL) has started. The global timing system has been used with LHCOSY to pulse klystrons for high power waveguide tests, but integrated tests of the controller systems with klystrons have not been started.

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